

Fig. 1

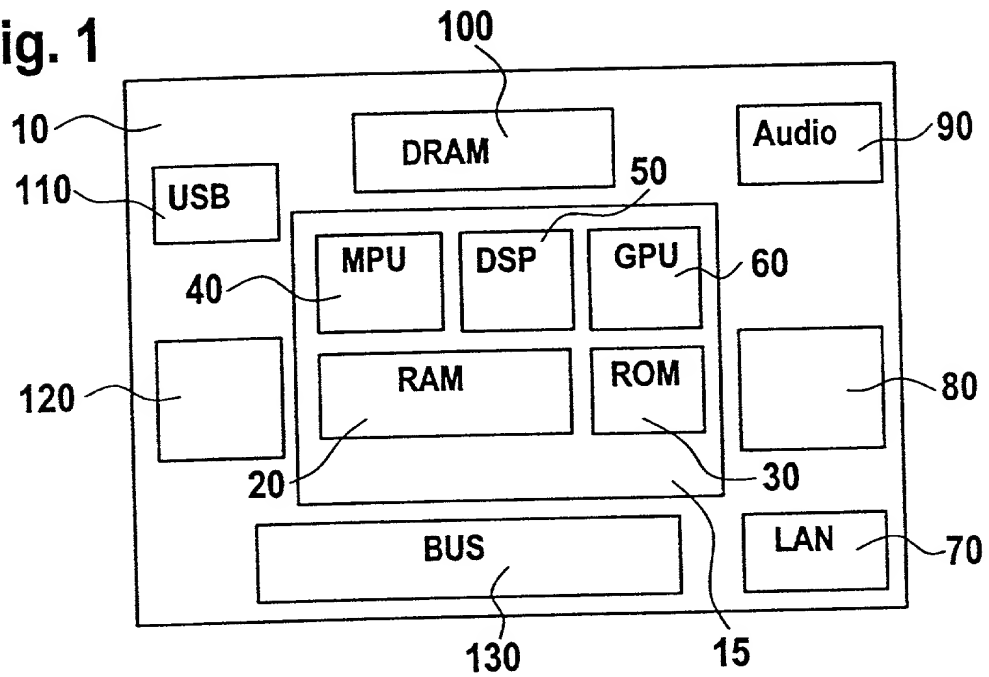


Fig. 2

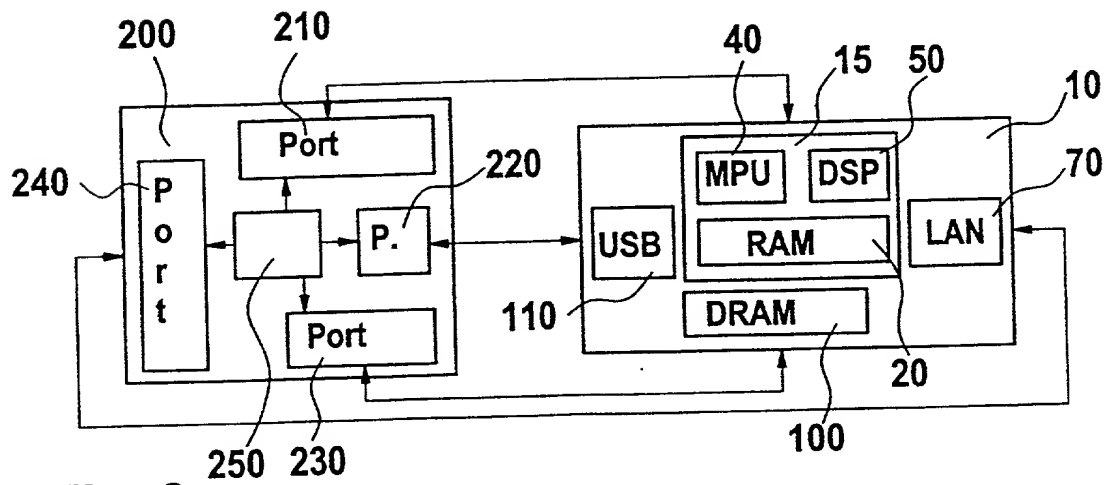


Fig. 3

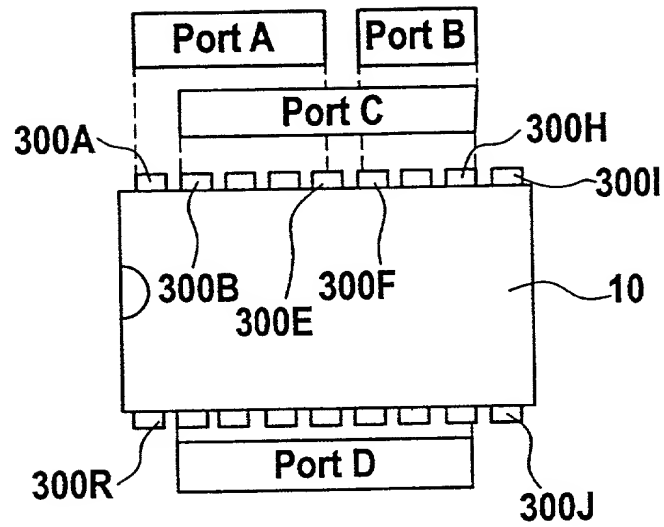


Fig. 4

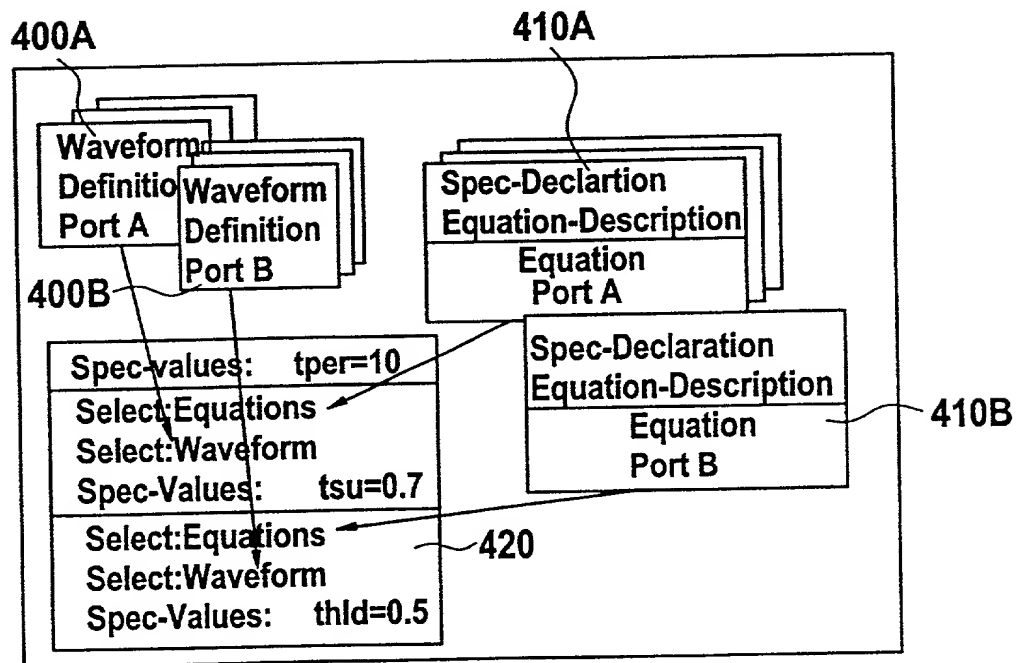


Fig. 5

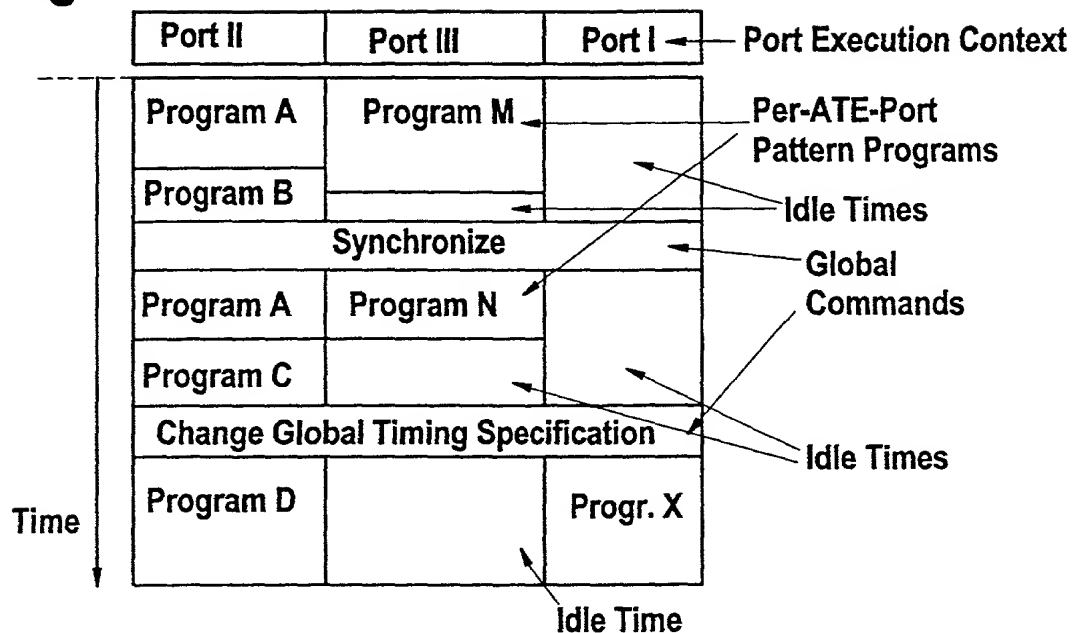
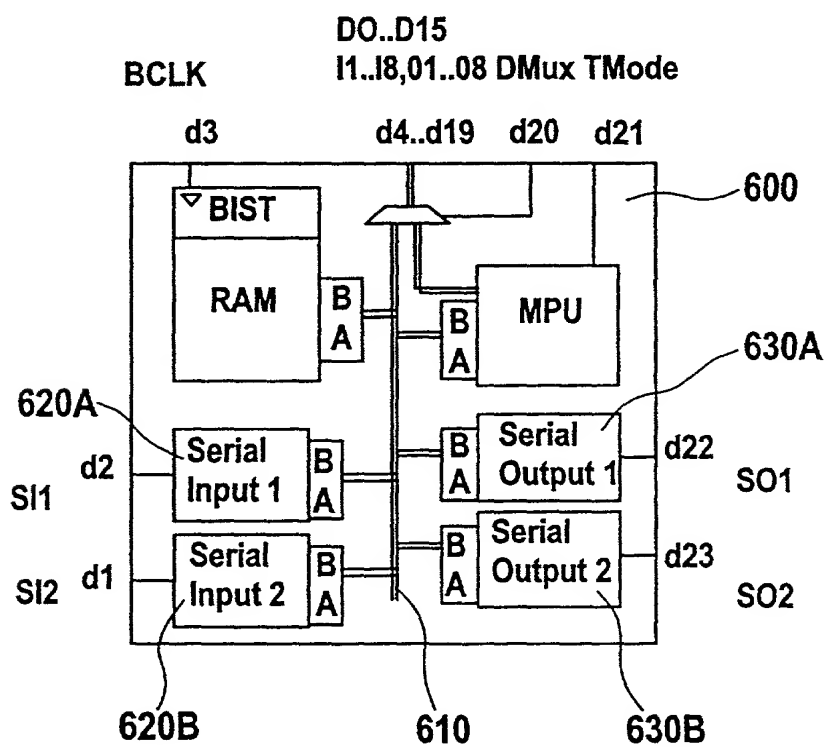


Fig. 6



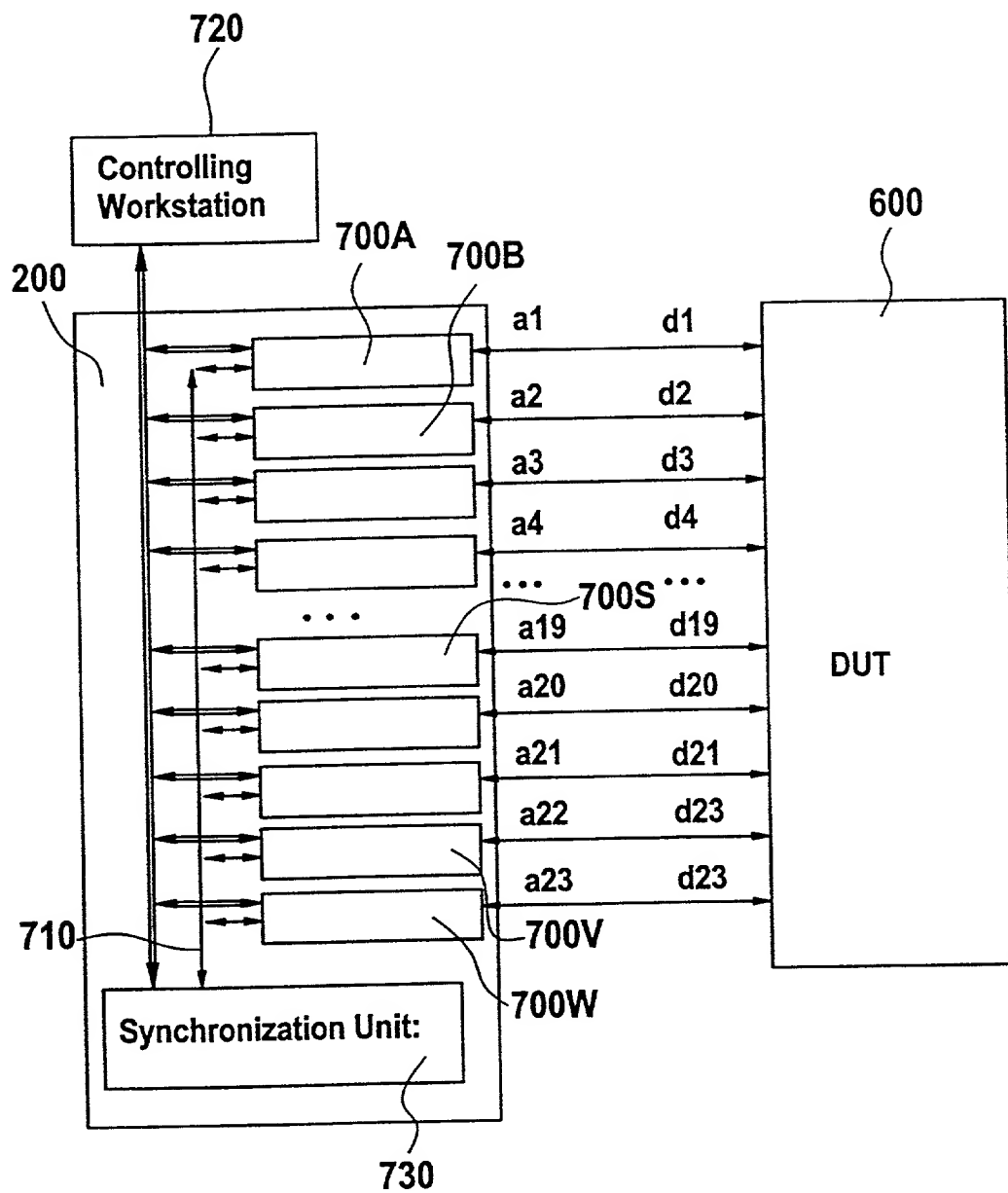


Fig. 7

Fig. 8

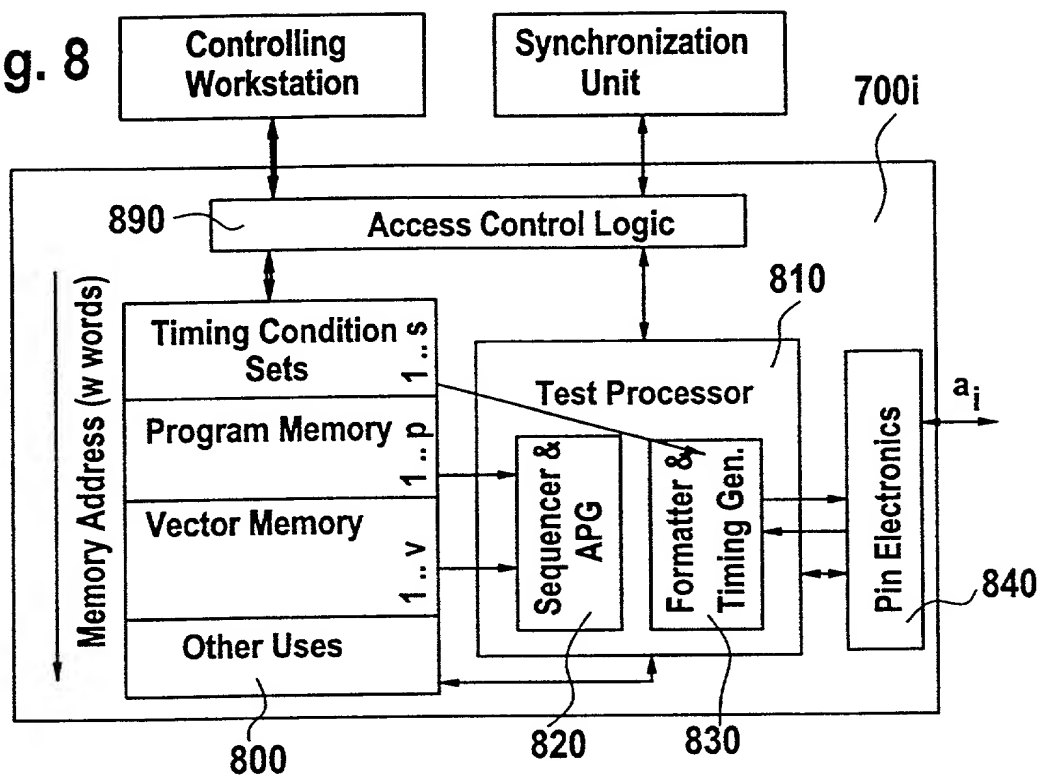
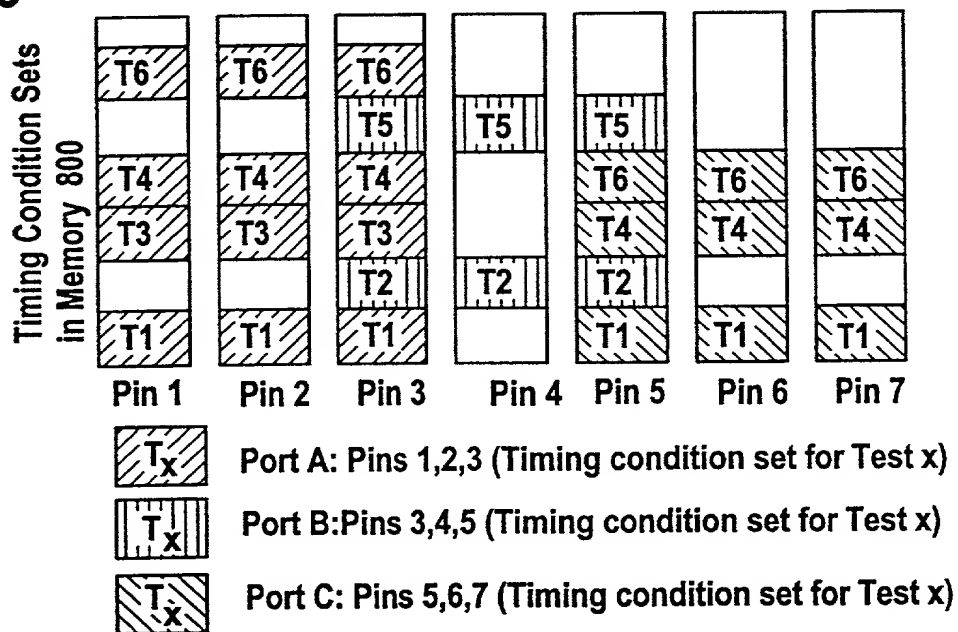


Fig. 9



Vec #	Pins				Sequencer Instruction
	D0	...	D15	Dmux	
0	X	...	X	0	CORE 1"SI1_Data" CORE 2"SO1_Data"
1	p		p	1	LOOP 10000; COREDATA 1
2	X		X	1	
3	p		p	1	COREDATA 2
4	X		X	1	
					LOOP END

Fig. 10